

SPICE Device Model Si7450DP

Vishay Siliconix

N-Channel 200-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

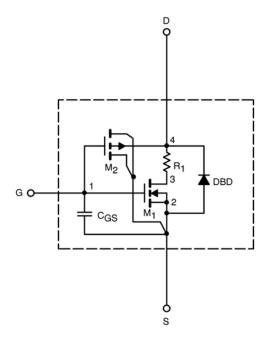
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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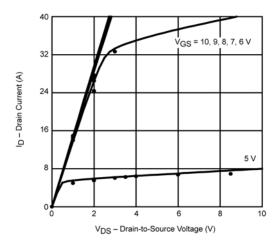
| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---------------------|--|-------------------|------------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | • | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | V_{DS} = V_{GS} , I_D = 250 μA | 3 | | V |
| On-State Drain Current ^a | I _{D(on)} | $V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$ | 74 | | Α |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V _{GS} = 10 V, I _D = 4 A | 0.068 | 0.065 | Ω |
| | | $V_{GS} = 6 \text{ V}, I_D = 4 \text{ A}$ | 0.072 | 0.070 | |
| Forward Transconductance ^a | g _{fs} | V_{DS} = 15 V, I_{D} = 5 A | 23 | 19 | S |
| Diode Forward Voltage ^a | V_{SD} | $I_S = 2.8 \text{ A}, V_{GS} = 0 \text{ V}$ | 0.76 | 0.75 | V |
| Dynamic ^b | <u> </u> | | • | | |
| Total Gate Charge | Q_g | V_{DS} = 100 V, V_{GS} = 10 V, I_{D} = 4 A | 35 | 34 | nC |
| Gate-Source Charge | Q_{gs} | | 7.5 | 7.5 | |
| Gate-Drain Charge | Q_{gd} | | 12 | 12 | |
| Turn-On Delay Time | t _{d(on)} | $V_{DD} = 100 \text{ V}, \text{ R}_L = 25 \Omega$ $I_D \cong 4 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_G = 6 \Omega$ $I_F = 2.8 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ | 27 | 14 | ns |
| Rise Time | t _r | | 39 | 20 | |
| Turn-Off Delay Time | $t_{\text{d(off)}}$ | | 39 | 32 | |
| Fall Time | t _f | | 55 | 25 | |
| Source-Drain Reverse Recovery Time | t _{rr} | | 70 | 70 | |

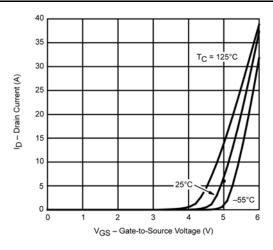
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

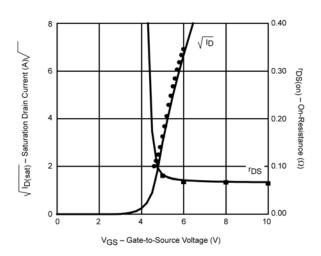


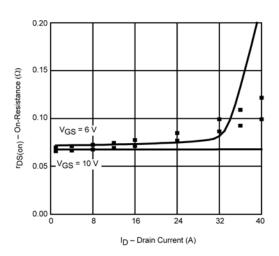
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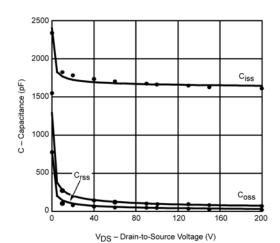
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

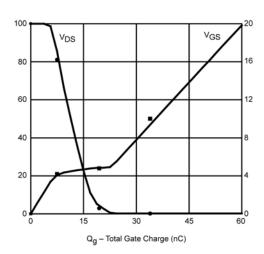












Note: Dots and squares represent measured data.



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